REMARKS

Entry of this Amendment if proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 3-22 are all the claims presently pending in the application. Claims 3-8, 18-19 and 22 have been amended to more particularly define the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 3-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata, et al. (U.S. Patent No. 5,880,500), in view of Wu (U.S. Patent No. 6,649,308).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as claimed in claim 3) is directed to a method for manufacturing a semiconductor device (e.g., an n-type metal oxide semiconductor field effect transistor (NMOSFET)).

The method includes implanting n-type impurities within an NMOSFET forming region during a formation of channel regions and n-type source/drain regions, and implanting boron ions for forming a channel region to adjust threshold voltage within the NMOSFET forming region divided by an element dividing region. Importantly, the method also includes implanting two different ions after the implantation of boron, including implanting arsenic ions in a semiconductor substrate at a first acceleration energy level which suppresses a reverse short channel effect to form arsenic ion implanted regions thereby forming the source/drain regions within the NMOSFET forming region, and after the implanting the arsenic ions, continuously implanting phosphorous ions in the arsenic ion implanted regions, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted region, and performing a heat treatment to activate the arsenic ions and the phosphorous ions

in the ion-implanted regions to form source/drain regions and buffer regions, the buffer regions including phosphorous ions and extending beyond the source/drain regions, thereby suppressing transient enhancement diffusion (TED) of a boron implanted region. The method also includes forming an NMOSFET having the source/drain.

In another aspect (e.g., as recited in claim 8 and similarly in claim 22), the claimed invention is directed to a method of manufacturing a semiconductor device, in which the first acceleration energy (e.g., arsenic ions) is no greater than 15keV and said second acceleration energy (e.g., phosphorus ions) is no greater than 10 keV.

Conventional methods of forming source/drain regions in a semiconductor device (e.g., an NMOSFET) include implanting arsenic at a high acceleration energy of about 50 keV in the source/drain region. However, as channel length and source/drain regions have become smaller, a reverse short channel effect has been realized in which the threshold voltage fluctuates largely for with a change in the length of the gate. The acceleration energy of implantation could be lowered to eliminate this reverse short channel effect, but this would result in an undesirable increase in p-n junction leakage current.

The claimed method, on the other hand, implants arsenic ions and, after the implanting the arsenic ions, continuously implants phosphorous ions in the arsenic ion implanted regions, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted region, and performing a heat treatment to activate the arsenic ions and the phosphorous ions in the ion-implanted regions to form source/drain regions and buffer regions, the buffer regions including phosphorous ions and extending beyond the source/drain regions, thereby suppressing transient enhancement diffusion (TED) of a boron implanted region.

The inventors found that implanting phosphorous into the arsenic implanted regions of the substrate helps to inhibit a leakage current. Thus, the claimed invention is able to implant arsenic at an acceleration energy (e.g., a low acceleration energy) which inhibits a reverse short channel effect without increasing the p-n junction leakage current (Application at page 14, lines 13-22).

II. THE IWATA AND WU REFERENCES

The Examiner alleges that Iwata would have been combined with Wu to form the invention of the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Iwata discloses a method of forming a semiconductor device in which phosphorous is implanted in a silicon substrate to form a first impurity diffusion region, and arsenic is later implanted to form a second impurity diffusion region (Iwata at Figure 1; col. 10, line 57-col. 11, line 15). Specifically, Iwata discloses a method in which first impurity regions 105 are formed by implanting phosphorous ions at an acceleration energy of 10-30 keV (Iwata at col. 11, lines 1-15). Thereafter, the impurities are activated at 850 to 900 °C (Iwata at col. 11, lines 59-64). Thereafter, third impurity regions 108 are formed by implanting arsenic ions at 20-40 keV (Iwata at col. 12, lines 34-40).

Wu discloses an ultra-short channel transistor in a semiconductor substrate includes a gate structure that is formed on the substrate. Side-wall spacers are formed on the side walls of the gate structure as an impurities-diffusive source. Source and drain regions are formed in the substrate. A metal silicide contact is formed on the top surface of the gate structure, and on the surface of the source and drain regions. Extended source and drain regions are formed beneath the side-wall spacers and connect next to the source and drain regions.

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions.

Specifically, Khouja is directed to a method of computing the power dissipated in a digital circuit, whereas the SDF publication is merely directed to a method of representing and interpreting timing data. Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, contrary to the Examiner's allegations, neither of these references teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the

Examiner has failed to make a prima facie case of obviousness.

Moreover, Applicant respectfully submits that neither Iwata, nor Wu, nor any combination thereof teaches or suggests a method of forming a semiconductor device in which arsenic is implanted at a first acceleration energy (e.g., to form source/drain regions) "*after said implanting said arsenic ions, continuously implanting phosphorous ions in the arsenic ion implanted regions, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted region*" , as recited, for example, in claim 3, nor "*wherein said first acceleration energy is no greater than 15keV and said second acceleration energy is no greater than 10 keV*", as recited in claim 8 and similarly in claim 22.

As noted above, unlike conventional methods, the inventors found that implanting phosphorous into the arsenic implanted regions of the substrate helps to inhibit a leakage current. Thus, the claimed invention is able to implant arsenic at an acceleration energy (e.g., a low acceleration energy) which inhibits a reverse short channel effect without increasing the p-n junction leakage current (Application at page 14, lines 13-22).

The Application explains that the inventors of the claimed invention found that when phosphorous ions are implanted into an arsenic implanted region, a subsequent heat treatment causes the phosphorous ions to diffuse shallower than phosphorous ions implanted without a previous arsenic implantation (Application at page 11, lines 1-5). This is because the point defects generated by the phosphorous ion implantation are absorbed by the amorphous silicon layer generated by the arsenic ion implantation, so that the diffusion of the phosphorous ion assisted by the point defects is weakened (Application at page 11, lines 6-10).

Therefore, the inventors have discovered that by implanting phosphorous after implanting arsenic, the distance between the amorphous silicon/ monocrystalline silicon interface and a p-n junction interface can be increased. This allows the arsenic implantation energy to be reduced to eliminate the reverse short channel effect, without causing the p-n junction leakage current to increase (Application at page 10, lines 15-22).

Clearly, neither Iwata nor Wu teach or suggest these novel features. Indeed, the Examiner asserts on page 5 of the Office Action:

"Regarding claim 8, Iwata et al. (figure 1) teach a method for manufacturing a semiconductor device comprising:

implanting arsenic ions in a semiconductor substrate (100) at a first acceleration energy level to form an arsenic ion implanted region (108) (column 11, lines 8-15)

implanting phosphorous ions in the arsenic ion implanted region (impurity diffusion region [108]) at a second acceleration energy level (column 10, line 66 - column 11, line 3) lower than the first acceleration energy level; and"

However, the process sequence of the above manufacturing steps is contrary to the claimed invention.

That is, according to the claimed invention, phosphorous ions are implanted after arsenic ions are implanted. Thus, Iwata teaches manufacturing steps that are reverse of the claimed invention.

In addition, Iwata teaches that arsenic ions are implanted after a high-melting-point metal silicide film is formed (Iwata at col. 11, lines 9-11), and that phosphorous ions are implanted after the gate electrode sidewall dielectric films are formed (Iwata at col. 10, line 67-col. 11, line 1). These passages in Iwata teach that implantation of phosphorous and arsenic ions are implemented as completely separate steps (e.g., see, the third embodiment of Iwata).

According to the claimed invention, on the other hand, implantation of phosphorus succeeds implantation of arsenic, which is completely different than the Iwata method.

According to the claimed invention, aresenic ions are implanted in a low implantation energy level to suppress the reverse short channel effect, and continuously phosphorus ions are implanted at a low implantation energy which is lower than the implantation energy of arsenic ions to form a concentration peak region of implanted ions within the arsenic ion implanted region.

Further, heat treatment is performed on the ion implanted regions for activation of the arsenic ions and phosphorus ions to form source/drain regions, thereby providing a NMOSFET having a suppressed reverse short channel effect, and a suppressed transient enhancement diffusion (TED) of the boron.

Iwata, merely teaches to protect from the short channel effect, which is not the same as a reverse channel effect.

Iwata clearly does not teach or suggest an object of the structure of the claimed invention which may suppress the transient enhancement diffusion (TED) of the boron

implanted in the channel region, and which may also suppress the reverse channel effect.

Further, Wu clearly does not teach or suggest the novel features of the claimed invention. Indeed, the Examiner merely relies on Wu as allegedly teaching implanting arsenic at a specific acceleration energy (Office Action at page 3).

However, nowhere does Wu teach or suggest implanting phosphorus ions after implanting the arsenic ions. Certainly, Wu does not teach or suggest implanting phosphorous ions in an arsenic ion implanted region at a second acceleration energy level lower than the first acceleration energy level (for implanting arsenic).

Further, neither Iwata nor Wu teach or suggest implanting arsenic at a first acceleration energy which is no greater than 15keV and implanting phosphorus in arsenic implanted regions at a said second acceleration energy which is no greater than 10 keV, as recited, for example, in claim 8, and similarly recited in claim 22.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 3-22, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 8/9/04

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Quang Vu Group Art Unit # 2811 at fax number (703) 872-9306 this 9th day of August, 2004.

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